

# Notice of Allowability

Application No.

09/903,227

Examiner

Hai L. Nguyen

Applicant(s)

BELL, DEBRA M.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendments filed on 11/01/04.
2. ☒ The allowed claim(s) is/are 1-49 and 74-84.
3. ☒ The drawings filed on 11 July 2001 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All b) ☐ Some\* c) ☐ None of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
  - \* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

## Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date \_\_\_\_\_
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

TIMOTHY P. CALLAHAN

SUPERVISORY PATENT EXAMINER

## **DETAILED ACTION**

### ***Response to Amendment***

1. The amendments received on 11/01/04 has been received and entered in the case. Applicant's arguments with respect to the previous prior art rejections mailed on 09/09/04 have been considered and found persuasive. In view of Applicant's amendments and arguments, the prior art rejections have been withdrawn. Therefore the case is found to be in allowance condition for the reasons as set for below.

## **REASON FOR ALLOWANCE**

2. The following is an examiner's statement of reasons for allowance:

The prior art of record fails to disclose or fairly suggest specific structural limitations, as recited in claim 1, such as a command react circuit (140, 500 in instant Figs. 4-5) connected to the selector (130) for enabling the selector to select the second delayed signal (116) based on a first state of a command signal (146) while the external and internal clock signals are synchronized (144, 145 are logic HI) to provide the internal clock signal (199) and for enabling the selector to select the first delayed signal (114) based on a second state of the command to provide the internal clock signal; and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest specific structural limitations, as recited in claims 5, 20, 28, 39, and 41, such as a command react circuit (140, 500 in instant Figs. 4-5) connected to the selector (130) for enabling the selector to select the second delayed signal (116) based on a first state of a command signal (146) to provide the internal clock signal (199)

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and for enabling the selector to select the first delayed signal (114) based on a second state of the command to provide the internal clock signal, wherein the command react circuit includes a first input for receiving a command signal (146), a second input for receiving a phase detect signal (145), and an output node responsive to the command and phase detect signals for providing a command set signal (122) to enable the selector to replace the first delayed signal (DLLCK0) with the second delayed signal (DLLCK1) when the command signal is activated (logic level Hi) while the external and internal clock signals (101, 155) are synchronized (144 is at logic level Hi), and to enable the selector to replace the second delayed signal with the first delayed signal when the phase detect signal is activated and the command signal is not activated; and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest specific structural limitations, as recited in claims 6, 13, 22, 30, 74, 79, and 82, and a method of operating delay locked loop, such as a command react circuit (140, 500 in instant Figs. 4-5) connected to the selector (130), the command react circuit including a first input for receiving a command signal (546), a second input for receiving a phase detect signal (544), and an output node responsive to the command and phase detect signals for providing a command set signal (522) to enable the selector to provide the internal clock signal based on the second delayed signal (116) when the command signal is activated, and to provide the internal clock signal based on the first delayed signal (114) when the command signal is deactivated; and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

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The prior art of record fails to disclose or fairly suggest specific structural limitations, as recited in claims 15 and 24, such as a command react circuit (140, 500 in instant Figs. 4-5) connected to the selector (130), the command react circuit including a first input for receiving a command signal (546), a second input for receiving a phase detect signal (544), and an output node responsive to the command and phase detect signals for providing a command set signal (522) to enable the selector to provide the internal clock signal based on the second delayed signal (116) when the command signal is activated, and to provide the internal clock signal based on the first delayed signal (114) when the command signal is deactivated; a phase detector (150) for comparing the external and internal clock signals to produce shifting signals (142, 143); a shift register (305 in instant Fig.3) for adjusting the first amount of delay and the second amount of delay based on the shifting signals when the external and internal clock signals are not synchronized (144 is at logic level Lo); and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

### *Conclusion*

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN   
November 8, 2004